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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/715,887 | 11/18/2003 | Paola Zuliani | 856063.755 | 3695 |

38106 7590 02/09/2005

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| EXAMINER | |
|---|---|
| THOMAS, TONIAE M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2822 | |

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/715,887 | ZULIANI ET AL. | |
| | Examiner | Art Unit | |
| | Toniae M. Thomas | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *6-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6 and 8-20* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Group II, claims 6-9, in the reply filed on 09 November is acknowledged. Claims 1-5 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

2. The amendment filed on 09 November 2004 canceled nonelected claims 1-5, and added claims 10-20. Currently, claims 6-20 are pending.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 6, 9, 10, and 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cremonesi et al. (US 6,268,247 B1) in view of Libera et al. (US 2002/00060349 A1).

The Cremonesi et al. patent (Cremonesi) discloses a floating-gate tunneling oxide (FLOTOX) electrically erasable programmable read-only memory (EEPROM) device (figs. 6-10 and accompanying text). The EEPROM device comprises a matrix of memory cells and external circuitry (col. 5, lines 16-20), wherein the external circuitry may include high voltage (HV) and low

voltage (LV) transistors (col. 5, lines 26-33). The matrix comprises rows and columns of memory cell; each cell comprising a first gate stack 3', which forms a selection transistor, and a second gate stack 2', which forms a floating gate storage transistor (fig. 10 and col. 6, lines 63-65). The first and second gate stacks comprise a first oxide layer 5, 6, 11, wherein layers 6 and 11 form gate oxide layers for the floating gate transistor and the selection transistor, respectively, and 5 forms a tunnel oxide layer for the floating gate transistor (fig. 10 and col. 5, lines 21-26); a first polysilicon layer 7 (fig. 10 and col. 5, lines 34-36); an interpoly dielectric layer 9 (fig. 10 and col. 5, lines 37-41); and a second polysilicon layer 8 (fig. 10 and col. 5, lines 44-48).

The selection transistor 3' is a non short-circuited double polysilicon selection transistor (non-DPCC - col. 6, line 66 - col. 7, line 1). Thus, there is no contact between the first and second polysilicon layers of the selection transistor. The Libera et al. patent (Libera) discloses a low resistance contact structure for a non-DPCC selection transistor of EEPROM cells in a non-DPCC process (fig. 5, par. 19, and par. 27 - par. 37). The contact structure 20, which comprises copper, connects the first polysilicon layer 10 to the second polysilicon layer 6 via an opening formed in the first polysilicon layer, interpoly dielectric layer 9, and second polysilicon layer 6 (fig. 5 and par. 33 - par. 34).

Cremonesi and Libera are from the same field of endeavor, FLOTOX EEPROM devices. Thus, the purpose for which Libera is relied upon would

have been recognized in the Cremonesi patent by one of ordinary skill in the art at the time the invention was made.

As stated above, the selection transistor disclosed in Cremonesi is a non-DPCC selection transistor. That is, in forming the selection transistor, a contact is not formed between the first and second polysilicon layers. Thus, complex process steps and expensive additional masks are required to provide a short-circuit between the first and second polysilicon layers of the selection transistor (Libera - par. 6, lines 1-5). It would have been obvious to one of ordinary skill in the, at the time, the invention was made, to modify Cremonesi in view of Libera, because the low resistance contact taught by Libera is particularly suited for non-DPCC selection transistors. Furthermore, the contact is cheaper and easier to make, as compared with contacts in conventional non-DPCC manufacturing processes.

4. Claims 8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cremonesi in view of Libera as applied to claim 6 above, and further in view of Dixit et al. (US 4,960,732).

Libera does not teach that the contact is a polysilicon contact, or that a transition layer is provided between the contact and polysilicon layers. The Dixit et al. patent (Dixit) discloses a contact 22 (figs. 1A-1D and accompanying text). The contact is made of a material selected from one of doped polysilicon and tungsten (col. 5, lines 9-13). The contact further comprises transition

layers 18, 20. Layer 18 forms an adhesion layer, whereas layer 20 forms a diffusion barrier layer (col. 4, lines 20-23 and lines 38-42).

As stated above, the contact disclosed in Cremonesi is a tungsten contact. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Cremonesi and Libera, by forming an adhesion layer and diffusion barrier layer between the tungsten contact and the polysilicon layers, as taught by Dixit, because an adhesion layer provides good adhesion between the polysilicon and tungsten (Dixit - col. 4, lines 20-23), and a barrier layer prevents the diffusion of silicon and impurity dopants (Dixit - col. 4, lines 38-42). Secondly, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Cremonesi and Libera using Dixit, by replacing the tungsten contact with one made from doped polysilicon, as taught by Dixit, because doped polysilicon is an art-recognized equivalent conductive material that is used to form contacts in semiconductor devices.

***Allowable Subject Matter***

5. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
07 February 2005

Mary Wilczewski
Primary Examiner